

AMENDMENT AND RESPONSE

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Serial No.: 10/033,156

Filing Date: 10/25/2001

Attorney Docket No. 125.020US01

Title: SEALED NITRIDE LAYER FOR INTEGRATED CIRCUITS

REMARKS

Applicant has reviewed the Office Action mailed on August 25, 2004 as well as the art cited. Claims 1-12 and 14-17 are pending in this application.

Rejections Under 35 U.S.C. § 103

Claims 1-12 were rejected under 35 USC § 103(a) as being unpatentable over Tu et al. (U.S. Patent No. 6,486,033) in view of Wu (U.S. Patent No. 5,679,601). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP 2143

Claim 1

Claim 1 is as follows:

1. (Previously presented) A method of forming a sealing nitride layer overlaying an oxide layer in a contact opening of an integrated circuit, the method comprising:

forming a second layer of nitride overlaying a first layer of nitride without any intervening layers between the first and second layers of nitride to form the sealing nitride layer, the second layer of nitride further overlaying and in contact with an exposed portion of a surface of a substrate in the contact opening and sidewalls of the contact opening; and

using reactive ion etching (RIE etch) without a mask to remove a portion of the second nitride layer adjacent the surface of the substrate in the contact opening to expose a portion of the surface of the substrate in the contact opening without removing portions of the second nitride layer covering the sidewalls of the contact opening.

As pointed out by the Examiner, the Tu et al. reference does not teach RIE etching without a mask. Moreover, the Applicant traverses the Examiner's assertion that the use of RIE

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etching without a mask would be obvious in light of Wu reference. The use of RIE etching without a mask would destroy intended purpose of the device in the Tu et al. reference and hence not be an obvious solution. For example, if an RIE without a mask is used to remove nitride 28 from the surface of the contact openings in the logic part of the circuit such as over contact region 44 (the logic part is shown on the left side of Figure 8 of the Tu et al. reference) the etch will also remove the portion of nitride 28 on all other horizontal surfaces such as over shallow trench isolation (STI) oxide 12, oxide 20 and the adjacent surface of substrate 10 because the nitride deposits to the same thickness and etches at the same rate on all horizontal surfaces. This is well known in the art of spacer formation. Also see paragraph [0027] of the present application. This would leave the surface without the continuous cover required to form a sealing nitride layer.

Contacts to the memory part of the circuit (shown on the right side of Figure 8 of the Tu et al. reference) are formed after interpoly oxide 50 has been deposited, column 4 lines 31-38 of the Tu et al. reference. They are formed using a mask "conventional photolithography and etching are used to form self aligned contact openings" column 4 lines 31-38 of the Tu et al. reference. The openings in the oxide formed by the photolithography would act as mask for any subsequent etch of the underlying nitride 28. The nitride 28 could only be reached by RIE without a mask after the RIE had removed the oxide 50 which would destroy the intended structure. If the maskless RIE were done before the deposition of oxide layer 50, then nitride 28 would be removed from horizontal surfaces such as those of STI 12 as described above for the logic part of the circuit leaving no sealing nitride layer. Accordingly, the Tu et al. reference does not teach or suggest the use of an RIE without a mask nor does the Tu et al. reference provide motivation to combine the cited references. Therefore, the obvious rejection of Claim 1 under section 103 is improper and the Applicant respectfully requests the withdrawal of the rejection.

Moreover, since dependant Claims 2-6 depend from and further define patentably distinct Claim 1, the Applicant also respectfully requests the withdrawal of these dependant claims. Since, the Applicant believes these dependant claims are allowable for the above reason, responses to all rejections to these claims may not have been put forth in this response. The

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Applicant, however, retains the right to respond to all said rejections if a further response is needed.

Claim 7

Claim 7, is as follows:

7. (Previously presented) A method of forming an integrated circuit, the method comprising:

- forming a layer of oxide over a surface of a substrate;
- forming a first layer of nitride overlaying the layer of oxide;
- forming a contact opening through the first layer of nitride and the oxide layer to expose a portion of the surface of the substrate;
- forming a second layer of nitride overlaying the first layer of nitride, the second layer of nitride also overlaying the exposed portion of the surface of the substrate in the contact opening and sidewalls of the contact opening; and
- using a reactive ion etch (RIE etch) without a mask on the substrate for a pre-determined amount of time to remove a portion of the second layer of nitride overlaying the surface of the substrate in the contact opening without removing the portions of the second nitride layer overlaying the sidewalls of the contact opening and without removing portions of the first nitride layer overlaying the oxide layer, wherein the oxide layer is sealed by the first and second nitride layers.

As illustrated Claim 7, also includes the element "using a reactive ion etch (RIE etch) without a mask..." As discussed in with regard to Claim 1, the Tu et al. reference does not teach or suggest the use of an RIE etch without a mask nor provide motivation to combine the cited references. Therefore, the Applicant respectfully requests the withdrawal of the rejection of Claim 7 under Section 103.

Moreover, since dependant Claims 8-16 depend from and further define patentably distinct Claim 7, the Applicant also respectfully requests the withdrawal of these dependant claims. Since, the Applicant believes these dependant claims are allowable for the above reason,

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responses to all rejections to these claims may not have been put forth in this response. The Applicant, however, retains the right to respond to all said rejections if a further response is needed.

Claims 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tu et al. in view of Wu, Leung et al. (US 6,573,548 B2) and Wolf et al.

Claim 14

Claim 14 is as follows:

14. (Previously presented) A method of forming semiconductor devices in an integrated circuit comprising:

forming a plurality of device regions of a first conductivity type in a substrate adjacent a surface of the substrate;

forming an oxide layer over a surface of a substrate;

patterning the oxide layer to expose pre-selected portions of the surface of the substrate;

forming a first layer of nitride overlaying the oxide layer and the exposed portions of the surface of the substrate;

implanting ions of a second conductivity type through the layer of nitride into the substrate to form device regions of the second conductivity type, wherein remaining portions of the oxide layer under the nitride layer selectively stop the ions from entering the substrate to selectively define edges of the device regions of the second conductivity type;

forming contact openings to expose a portion of each of the device regions of the first and second conductivity type in the substrate;

forming a second layer of nitride over the first layer of nitride, the second layer of nitride also overlaying the exposed portions of each of the device regions in their associated contact openings and sidewalls of each of the contact openings; and

exposing the substrate to a reactive ion etch (RIE etch) for a pre-determined amount of time to remove portions of the second layer of nitride adjacent a surface of each device region in an associated contact opening, wherein the substrate is not exposed to the RIE etch long enough

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to remove all of the portions of the second nitride layer overlaying the respective sidewalls of each of the contact openings and portions of the first layer of nitride overlaying the oxide layer so that the oxide layer remains sealed by the first and second layers of nitride.

Claim 14 include several aspects not taught or suggested in any of the cited art reference alone or in combination. For example, Claim 14 includes an REI etch type not taught or suggested by the Tu et al. reference for the reasons as set out in response to the rejection of Claim 1.

The Examiner is also incorrect in asserting that it would be obvious to implant through the nitride layer because it is known to implant through surface layers to provide a barrier for metals and other impurities. In the Tu et al. reference, the nitride layer that the Examiner identifies as the first nitride layer of the claim is etched to form spacers on the sides of the gates (column 4 lines 20-25 of the Tu et al. reference). It is well known that the purpose of spacers formed on the sides of gates is to define the edges of the implanted sources and drains at a desired distance from the gates. To accomplish this goal, the spacers must be formed before the source and drain implants are done and the remaining spacer material must block penetration of the implants into the surface of the semiconductor substrate. Thus it would not be possible to implant through nitride layer 24 of Tu et al. reference. Accordingly, the Tu et al. reference does not teach or suggest implanting through the nitride layer nor provide motivation to combine the references.

For the above reasons, the Applicant respectfully requests the withdrawal of the rejection of Claim 14 under section 103. Moreover, since dependant Claims 15-17 depend from and further define patentably distinct Claim 14, the Applicant also respectfully requests the withdrawal of these dependant claims. Since, the Applicant believes these dependant claims are allowable for the above reason, responses to all rejections to these claims may not have been put forth in this response. The Applicant, however, retains the right to respond to all said rejections if a further response is needed.

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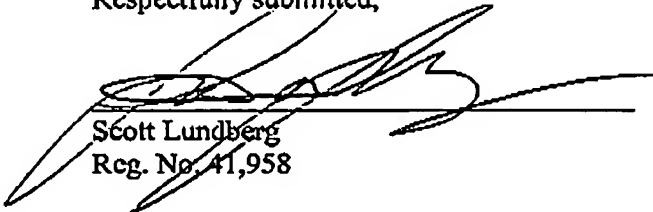
CONCLUSION

Applicant respectfully submits that claims 1-12 and 14-17 are in condition for allowance and notification to that effect is earnestly requested. If necessary, please charge any additional fees or credit overpayments to Deposit Account No. 502432.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at 612-455-1690.

Respectfully submitted,

Date: 11-24-04



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